REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. Made changes to table I, figure 1, figure 3, and figure 4. Editorial changes throughout.	1990 JUNE 28	

REV																									
SHEET																									
REV																									
SHEET																									
REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A										
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14										

PMIC N/A	PREPARED BY Kirk C. Officer	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	
STANDARDIZED MILITARY DRAWING	CHECKED BY Charles E. Besore	MICROCIRCUITS, LINEAR, CMOS, 14-BIT, A/D CONVERTER, MONOLITHIC SILICON	
THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	APPROVED BY Thomas L. Poelking		
	DRAWING APPROVAL DATE 04 AUGUST 1989	SIZE A	CAGE CODE 67268	5962-89674
AMSC N/A	REVISION LEVEL A	SHEET 1 OF 14	

DESC FORM 193
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60911

5962-E1711

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-89674	01	Q	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function	INT test
01	CS5014-S	14-bit CMOS A/D converter, 14.25 µs	±1.5 LSB
02	CS5014-T	14-bit CMOS A/D converter, 14.25 µs	±0.5 LSB

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
Q	D-5 (40-lead, 2.096" x .620" x .225"), dual-in-line package
X	C-5 (44-terminal, .662" x .662" x .120"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Positive digital supply voltage range ($+V_D$)	-0.3 V dc to +6.0 V dc 2/
Negative digital supply voltage range ($-V_D$)	+0.3 V dc to -6.0 V dc
Positive analog supply voltage range ($+V_A$)	-0.3 V dc to +6.0 V dc
Negative analog supply voltage range ($-V_A$)	+0.3 V dc to -6.0 V dc
Analog ground (AGND) to digital ground (DGND)	±0.5 V dc
Input current, any pin except supplies	±10 mA 3/
Analog input voltage range (A_{IN} and V_{REF} pins)	$-V_A - 0.3$ V dc to $+V_A + 0.3$ V dc
Digital input voltage range	-0.3 V dc to $+V_D$ + 0.3 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+260°C
Junction temperature (T_J)	+195°C
Power dissipation (P_D):	
Case Q	1500 mW
Case X	1100 mW
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case Q	+45°C/W
Case X	+60°C/W

1/ All voltages referenced to AGND and DGND tied together.
2/ In addition, $+V_D$ must not be greater than $+V_A$ + 0.3 V dc.
3/ Transient currents of up to 100 mA will not cause latch-up.

1.4 Recommended operating conditions. 1/

Ambient operating temperature range (T_A)	-55°C to +125°C
Positive digital supply voltage range ($+V_D$)	+4.5 V dc to $+V_A$ V dc 2/
Negative digital supply voltage range ($-V_D$)	-4.5 V dc to -5.5 V dc
Positive analog supply voltage range ($+V_A$)	+4.5 V dc to +5.5 V dc
Negative analog supply voltage range ($-V_A$)	-4.5 V dc to -5.5 V dc
Digital ground (DGND)	0 V dc
Analog ground (AGND)	0 V dc
Digital input low voltage range (V_{IL})	-0.3 V dc to +0.8 V dc
Digital input high voltage range (V_{IH})	+2.0 V dc to $+V_D$
Analog reference input voltage (V_{REF})	+4.5 V dc
Analog input voltage range:	
Unipolar mode	AGND to $+V_{REF}$
Bipolar mode	$-V_{REF}$ to $+V_{REF}$

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

1/ All voltages referenced to AGND and DGND tied together.
2/ In addition, $+V_D$ must not be greater than $+V_A$ + 0.3 V dc.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or B using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C < T_A < +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Resolution for which no missing codes is guaranteed	RES	1/	All	1, 2, 3	14		Bits
Integral linearity error	INL	1/ 2/	01	1, 2, 3		±1.5	LSB
			02			±0.5	
Differential linearity error	DNL	1/ 2/	All	1, 2, 3		±0.5	LSB
Full-scale error	FSE	1/ 2/	All	1, 2, 3		±1.0	LSB
Full-scale error drift	$dFSE/d_t$	1/ 2/ 3/ 4/	All	2, 3		±1.0	LSB
Unipolar offset error	VOFF	1/ 2/	01	1, 2, 3		±1.0	LSB
			02			±0.75	
Unipolar offset error drift	$dVOFF/d_t$	1/ 2/ 3/ 4/	All	2, 3		±0.5	LSB
Bipolar offset error	BOFF	1/ 2/	01	1, 2, 3		±1.0	LSB
			02			±0.75	
Bipolar offset error drift	$dBOFF/d_t$	1/ 2/ 3/ 4/	All	2, 3		±1.0	LSB
Bipolar negative full-scale error	BNFSE	1/ 2/	01	1, 2, 3		±1.5	LSB
			02			±1.0	
Bipolar negative full-scale error drift	$dBNFSE/d_t$	1/ 2/ 3/ 4/	All	2, 3		±1.0	LSB
Analog input capacitance in fine charge mode	C_{IN}	Unipolar mode $T_A = +25°C$ 1/ 3/	All	4		375	pF
		Bipolar mode $T_A = +25°C$ 1/ 3/				220	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C < T_A < +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Peak harmonic or spurious noise	S/PN	1 kHz input, full scale 1/ amplitude, bipolar mode 2/	01	4, 5, 6	85		dB
			02		94		
		12 kHz input, full scale 1/ amplitude, bipolar mode 2/	01		80		
			02		84		
Signal to noise ratio	S/(N+D)		01	4, 5, 6	80		dB
			02		82		
Digital input voltage (HOLD, CLKIN, CAL, INTRLV, BW, RST, BP/UP, AO, RD, CS)	V_{IH}	5/ 6/	All	1, 2, 3	2.0		V
	V_{IL}		All			0.8	
Digital input current	I_{IN}	5/ 6/	All	1, 2, 3		±10	µA
Digital output voltage (D0-D15, SDATA, SCLK, EOC, EOT)	V_{OL}	Logic "0", 5/ 6/ I_{SINK} = -1.6 mA	All	1, 2, 3		0.4	V
	V_{OH}	Logic "1", 5/ 6/ I_{SOURCE} = 100 µA			$+V_D$ -1.0		
High impedance state output current	I_Z	Pins D_0 to D_{15} only 5/ 6/	All	1, 2, 3		±10	µA
Conversion time	t_C	1/ 6/ 7/	All	9, 10, 11		14.25	µs
Acquisition time	t_{ACQ}	T_A = +25°C 1/ 2/ 3/ 8/	All	9		3.75	µs
Throughput	t_{PUT}	1/ 6/ 7/	All	9, 10, 11	55.6		kHz
Positive analog supply current	$+I_A$	$+V_A$, $+V_D$ = 5.5 V 6/ 9/ $-V_A$, $-V_D$ = -5.5 V	All	1, 2, 3		19.0	mA
Negative analog supply current	$-I_A$	$+V_A$, $+V_D$ = 5.5 V 6/ 9/ $-V_A$, $-V_D$ = -5.5 V	All	1, 2, 3		19.0	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C < T_A < +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Positive digital supply current	$+I_D$	$+V_A$, $+V_D$ = +5.5 V 6/ 9/ $-V_A$, $-V_D$ = -5.5 V	All	1, 2, 3		6.0	mA
Negative digital supply current	$-I_D$	$+V_A$, $+V_D$ = +5.5 V 6/ 9/ $-V_A$, $-V_D$ = -5.5 V	All	1, 2, 3		6.0	mA
Master clock frequency 10/	f_{CLK}	$T_A = -55°C$ Internally generated CLKIN = 0 V $+V_D$, $+V_A$ = +4.5 V $-V_D$, $-V_A$ = -4.5 V	All	11	1.75		MHz
$\overline{HOLD}$ pulse width	t_{HPW}	See figure 4 5/ 6/ 11/	All	9, 10, 11	$\frac{1}{f_{CLK}} + 50$	t_C	ns
Data delay time	t_{DD}	See figure 4 5/ 6/ 11/	All	9, 10, 11		100	ns
$\overline{EOC}$ pulse width	t_{EPW}	See figure 4 5/ 6/ 11/	All	9, 10, 11	$\frac{4}{f_{CLK}} - 20$		ns
CAL, $\overline{INTRLV}$ to $\overline{CS}$ low setup time	t_{CS}	See figure 5 5/ 6/ 11/	All	9, 10, 11	20		ns
A0 to $\overline{CS}$ and $\overline{RD}$ low setup time	t_{AS}	See figure 5 5/ 6/ 11/	All	9, 10, 11	20		ns
$\overline{CS}$ or $\overline{RD}$ high to A0 invalid hold time	t_{AH}	See figure 5 5/ 6/ 11/	All	9, 10, 11	50		ns
$\overline{CS}$ high to CAL, $\overline{INTRLV}$ invalid hold time	t_{CH}	See figure 5 5/ 6/ 11/	All	9, 10, 11	50		ns
$\overline{CS}$ low to data valid access time	t_{CA}	$\overline{RD}$ = logic "0" See figure 5 5/ 6/ 11/	All	9, 10, 11		150	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
$\overline{RD}$ low to data valid access time	t_{RA}	$\overline{CS}$ = logic "0" See figure 5 5/ 6/ 11/	All	9, 10, 11		150	ns
Output float delay	t_{FD}	See figure 5 5/ 6/ 11/	All	9, 10, 11		140	ns
SDATA to SCLK rising setup time	t_{SS}	See figure 6 5/ 6/ 11/	All	9, 10, 11	$\frac{2}{f_{CLK}} - 50$		ns
SCLK rising to SDATA hold time	t_{SH}	See figure 6 5/ 6/ 11/	All	9, 10, 11	$\frac{2}{f_{CLK}} - 100$		ns

1/ $+V_A$, $+V_D$ = +5.0 V; $-V_A$, $-V_D$ = -5.0 V; V_{REF} = +4.5 V dc; f_{CLK} = 4 MHz; analog source impedance = 200 ohms; error tests are done after calibration at the temperature of interest.

2/ Synchronous sampling mode ($\overline{EOT}$ connected to $\overline{HOLD}$), interleave disabled.

3/ This parameter shall be measured only for initial characterization, and after process or design changes which may affect this parameter.

4/ Total drift over -55°C to +125°C range since calibration at power-up at +25°C.

5/ $+V_A$, $+V_D$ = +5.0 V dc ±10 percent; $-V_A$, $-V_D$ = -5.0 V dc ±10 percent.

6/ This parameter is guaranteed, if not tested, at T_A = +25°C. This parameter is tested at T_A = -55°C and +125°C.

7/ Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{EOC}$.

8/ Acquisition time is the time allowed by the converter for acquisition of the input voltage prior to conversion.

9/ All outputs unloaded; All inputs swinging between $-V_D$ and 0 V dc.

10/ Externally supplied maximum clock frequency is 4 MHz. Analog parametric measurements are done with the maximum frequency external clock (see footnote 1/).

11/ Inputs: logic "0" = 0 V; logic "1" = $+V_D$; C_L = 50 pF.

Device types	01 and 02	
Case outlines	Q	X
Terminal number	Terminal symbol	
1	$\overline{HOLD}$	$\overline{HOLD}$
2	D_0	D_0
3	D_1	D_1
4	D_2	D_2
5	D_3	D_3
6	D_4	D_4
7	D_5	D_5
8	D_6	D_6
9	D_7	NC
10	DGND	D_7
11	$+V_D$	DGND
12	D_8	$+V_D$
13	D_9	NC
14	D_{10}	D_8
15	D_{11}	NC
16	D_{12}	D_9
17	D_{13}	D_{10}
18	D_{14}	D_{11}
19	D_{15}	D_{12}
20	$\overline{CLKIN}$	D_{13}
21	$\overline{CS}$	D_{14}
22	$\overline{RD}$	D_{15}

Device types	01 and 02	
Case outlines	Q	X
Terminal number	Terminal symbol	
23	AO	CLKIN
24	BP/$\overline{UP}$	$\overline{CS}$
25	$+V_A$	$\overline{RD}$
26	AIN	AO
27	AGND	BP/$\overline{UP}$
28	V_{REF}	$+V_A$
29	REFBUF	AIN
30	$-V_A$	AGND
31	TST	V_{REF}
32	RST	REFBUF
33	BW	NC
34	$\overline{INTRLV}$	$-V_A$
35	CAL	TST
36	$-V_D$	RST
37	$\overline{EOT}$	BW
38	$\overline{EOC}$	$\overline{INTRLV}$
39	SCLK	CAL
40	SDATA	$-V_D$
41	---	$\overline{EOT}$
42	---	$\overline{EOC}$
43	---	SCLK
44	---	SDATA

FIGURE 1. Terminal connections.

Function	$\overline{HOLD}$	$\overline{CS}$	CAL	INTRLV	$\overline{RD}$	A0	RST
Hold and start convert		X	X	X	X	See note	0
Initiate burst calibration	X	0	1	X	X	See note	0
Stop burst cal and begin track	1	0	0	X	X	See note	0
Initiate interleave calibration	X	0	X	0	X	See note	0
Terminate interleave cal	X	0	X	1	X	See note	0
Read output data	X	0	X	X	0	1	0
Read status register	1	0	X	X	0	0	0
High impedence data bus	X	1	X	X	X	See note	X
High impedence data bus	X	X	X	X	1	See note	X
Reset	X	X	X	X	X	X	1
Reset	0	0	X	X	X	0	X

NOTE: The status of A0 is not critical to the operation specified. However, A0 should not be low with $\overline{CS}$ and $\overline{HOLD}$ low, or a software reset will result.

FIGURE 2. Truth table.

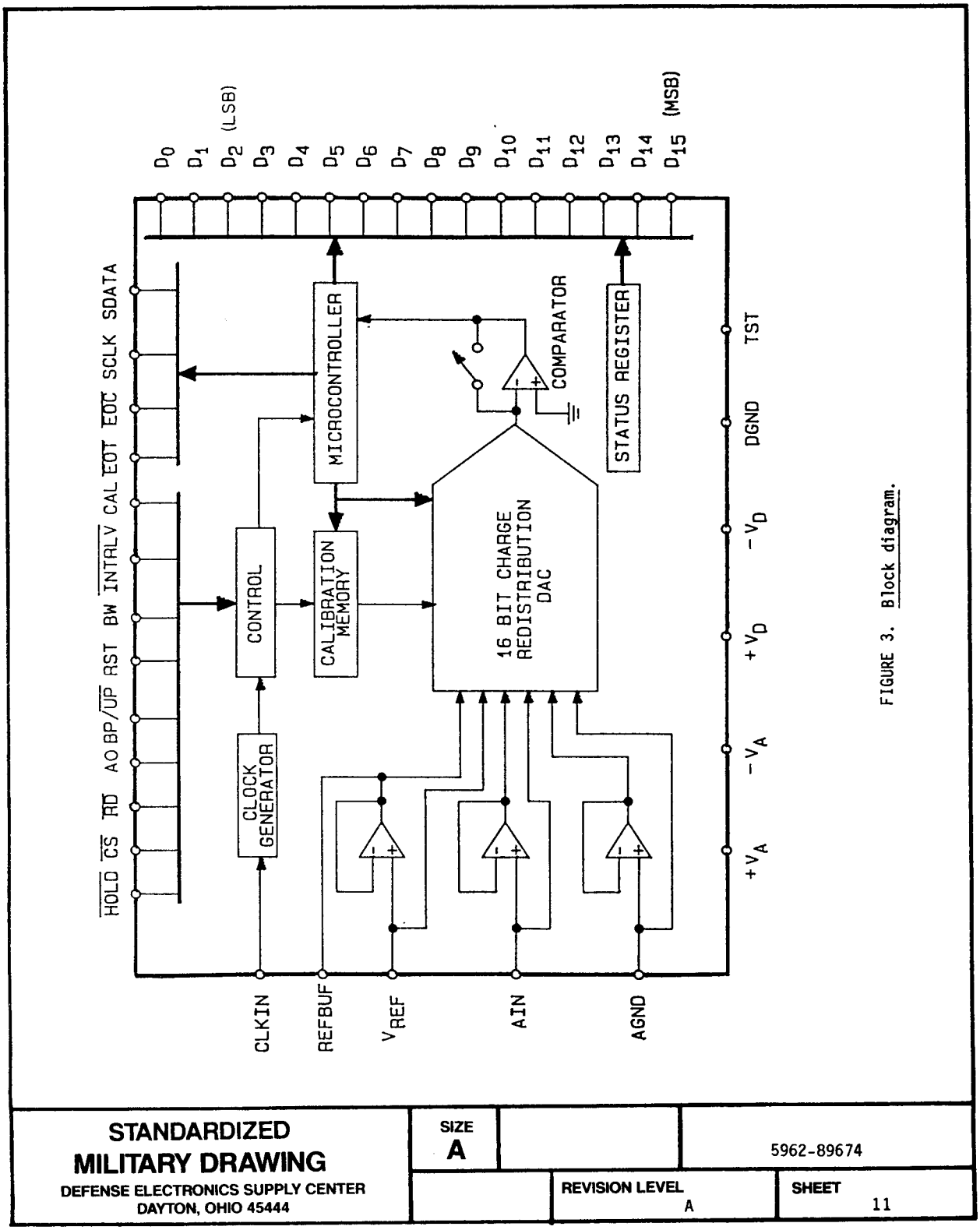

FIGURE 3. Block diagram.

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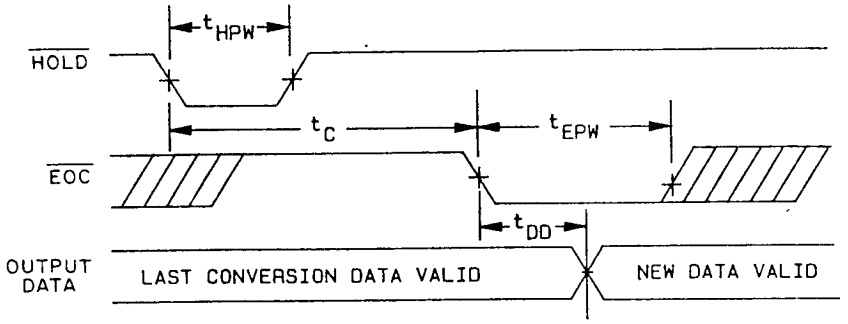

FIGURE 4. Conversion timing.

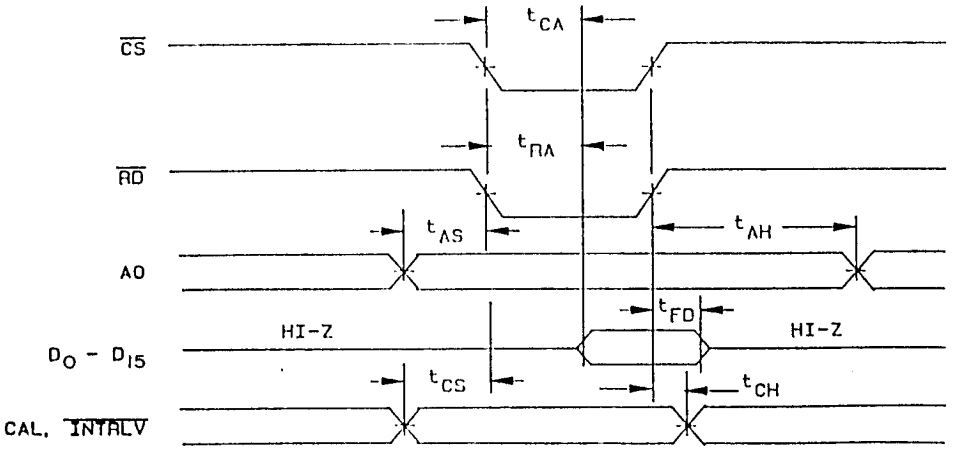

FIGURE 5. Read and calibration control timing.

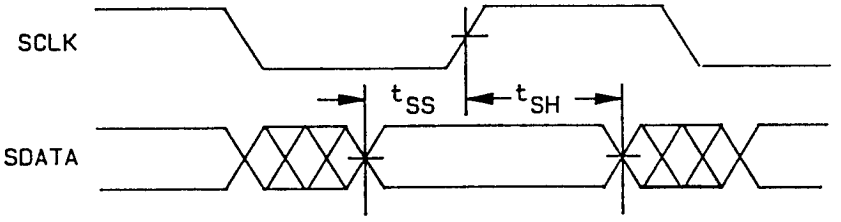

FIGURE 6. Serial output timing.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirement	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1, 4
Final electrical test parameters (method 5004)	1*, 2, 3, 4, 5, 6, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 5, 6, 10, 9**, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3

* PDA applies to subgroup 1.
** Subgroup 9 will be guaranteed if not tested.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or B using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved source of supply. An approved source of supply is listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendor listed in MIL-BUL-103 has agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved source of supply listed below is for information purposes only and is current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8967401QX	0A384	CS5014-SD14B
5962-8967401XX	0A384	CS5014-SE14B
5962-8967402QX	0A384	CS5014-TD14B
5962-8967402XX	0A384	CS5014-TE14B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0A384	Crystal Semiconductor P.O. Box 17847 4210 South Industrial Drive Austin, TX 78760